ML7C964A

VME Interface Component

The ML7C964 is a VME interface component, pin-compatible with the now-discontinued Cypress CY7C964. The ML7C960 VME controller in concert with ML7C964 interface chips provides a simple VME interface solution.

Feature Summary

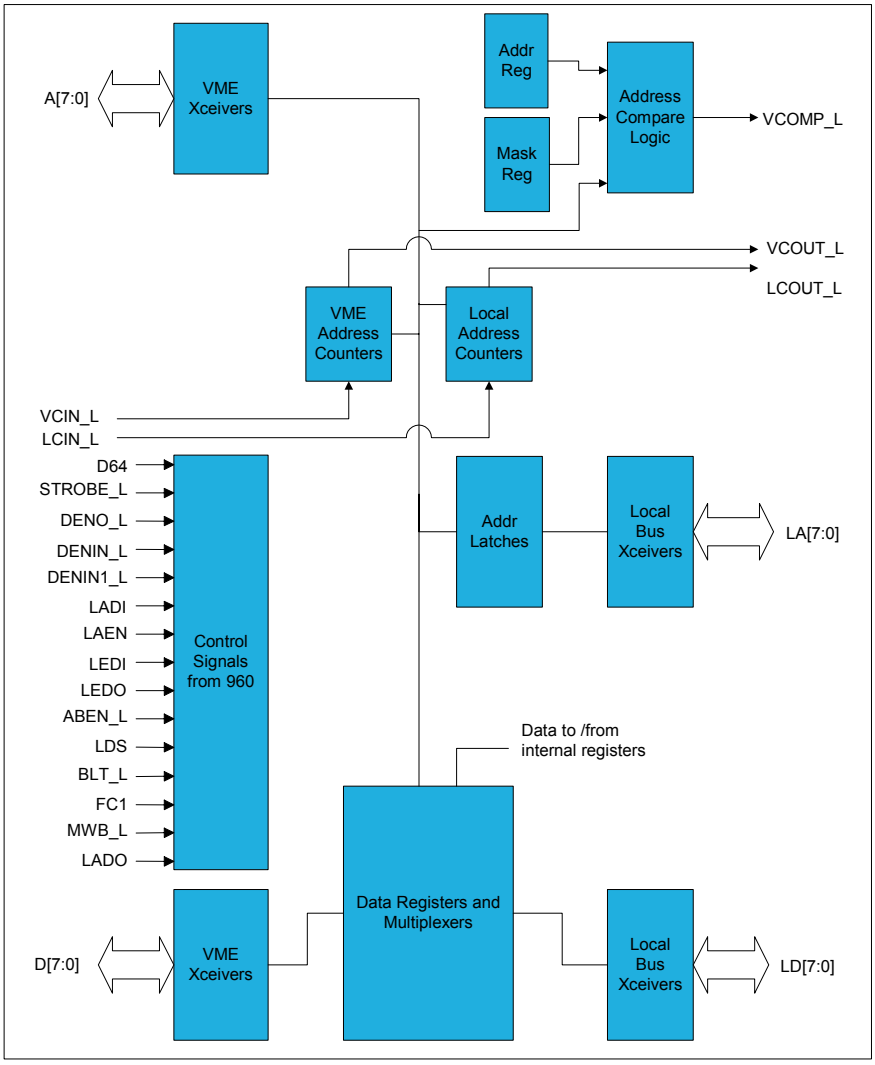
- High-current drivers for direct connection to VME address and data bus signals
- Cascadable to support multiple VME widths
- VME address matching
- Address counters for block transfers and local bus DMA.
- Supports all standard (Rev. C) VMEbus transactions
- 80-Mbyte-per-second block transfer rates
- Multiplexers for D64 support
- 64 pin PLCC package

Applications

VME64 has been widely used in industrial and military applications. The ML7C964 with the ML7C960 provides an integrated solution for VME and VME64 Slave devices.

The Millogic synthesizable core for the ML7C964 has been widely used to generate functional replacements for the Cypress CY7C964. The ML7C964 now provides a direct chip level replacement, requiring no printed circuit board changes.

Block Diagram



General Description

The ML7C964 is a byte-slice VME address and data interface. Millogic also provides the ML7C960, a pin compatible replacement device for the CY7C960 chips. The ML7C964 together with the ML7C960 provide a complete VME slave interface solution.

The ML7C964 is cascadable to support D8, D16, D32, MD32 and D64 data transfers. It can also support A16, A24, A32, A40, A64 addressing modes. Single-cycle and block-transfer read and write cycles, Read-Modify-Write cycles and Address-only cycles are all supported.

General Description

(continued)

The ML7C964 contains three address counters to support both master and slave block transfers. One counter supplies the local address during master block transfer operations, A second counter provides the local address during slave block transfers, and also serves as the address latch for non-block transfer slave operations. The third counter provides the VME address during VME master block transfers.

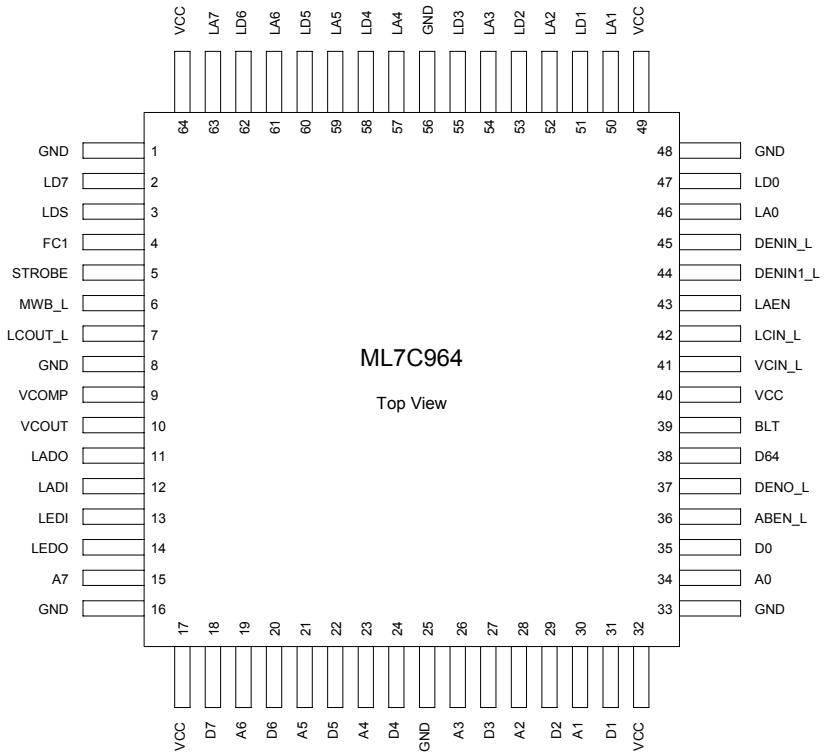
The address comparison logic comprises a base address register, a mask register. The VCOMP_L output is driven low when the VME address bits selected by the mask register match the corresponding bits in the base address register.

In D64 operation, data are transferred over both the VME A and D pins. The ML7C964 handles the sequencing and routing of data between the local data (LD) pins and the A and D pins appropriately.

ML7C964—CY7C964 A Comparison

Functionally, the ML7C964 and CY7C964 are the equivalent. With the ML7C964, in D64 mode (when data are driven on both the D and A signals,) the VME drive current limit to is reduced to 20 ma per pin.

Pin Configuration



Package - 64 pin PQFP

Pin Description

Signal	Signal Direction	Description
A(7:0)	Bidir	VME address
D(7:0)	Bidir	VME data
LA	Bidir	Local address bus
LD	Bidir	Local data bus
LCOUT_L	Out	Local address counter enable out
VCOUT_L	Out	VME address counter enable out
VCOMP_L	Out	VME address compare out
D64	Input	ML7C960 interface - Informs external hardware D64 VME block xfer in progress
STROBE_L	Output	ML7C960 interface - Used during INIT to load 964 regs
DENO_L	Input	ML7C960 interface - Data Enable Out - Enables VME data drivers
DENIN_L	Input	ML7C960 interface - Data Enable In; used with DENIN1_L and SWDEN_L
DENIN1_L	Input	ML7C960 interface - Data Enable In; used with DENIN_L and SWDEN_L
LADI	Input	ML7C960 interface - Latch Address In
LAEN	Input	ML7C960 interface - Local Address Enable
LEDI	Input	ML7C960 interface - Latch Enable Data In
LEDO	Input	ML7C960 interface - Latch Enable Data Out
ABEN_L	Input	ML7C960 interface - Address Bus Enable; enables data onto VME address bus for D64 cycles
LDS	Input	Local Data Select; used during mux-ed data VME transactions and INIT
LCIN_L	Input	Local address counter enable in
VCIN_L	Input	VME address counter enable in
BLT_L	Input	Block transfer enable
FC1	Input	Function code 1
MWB_L	Input	Module Wants Bus – local bus requesting VME
LADO	Input	Latch Address Out

Recommended Operating Conditions

Operating Conditions

Parameter	Description	Test Conditions	Value	Units
V_{CC}	Operating power supply		5 +/- 10%	V
T_J	Junction Temperature		-40 to 125	°C

DC Specifications—All Inputs

Parameter	Description	Test Conditions	Value	Units
V_{IH}	Minimum High-level Input Voltage		2.2	V
V_{IL}	Maximum Low-level Input Voltage		0.8	V
$I_{IH\text{-}max}$	Maximum High-level Input Current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{IH\text{-}min}$	Minimum High-level Input Current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{IL\text{-}max}$	Maximum Low-level Input Current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{IL\text{-}min}$	Minimum Low-level Input Current	V_{IN} = GND; 50K pullup	-20	µA

DC Specifications—VME D Outputs

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -3ma	2.4	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 40ma	0.6	V

DC Specifications—VME A Outputs (D64 mode)

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -3ma	2.4	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 20ma	0.6	V

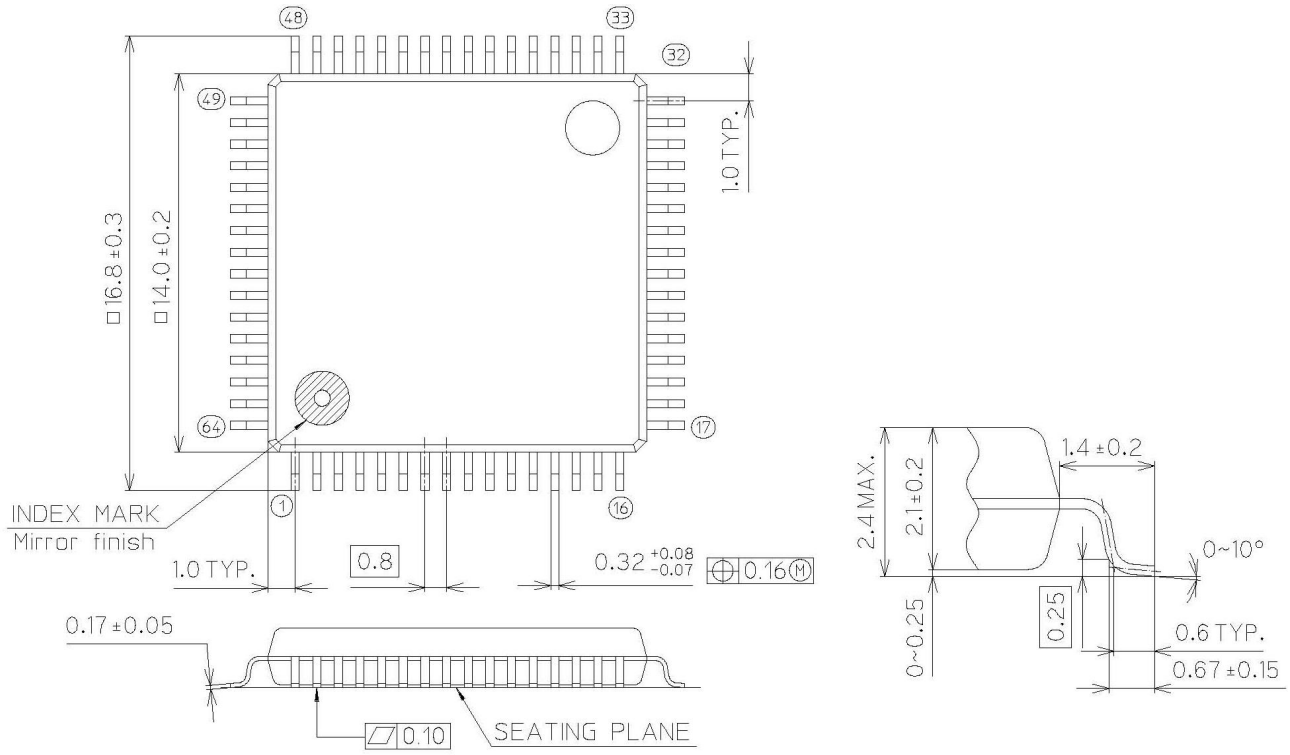
DC Specifications—All Other Outputs

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -8ma	2.8	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 8ma	0.4	V

DC Specifications—All Tristate Outputs—Leakage currents

Parameter	Description	Test Conditions	Value	Units
$I_{OZH\text{-}max}$	Max high-level leakage current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{OZH\text{-}min}$	Minimum pulldown current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{OZL\text{-}max}$	Max low-level leakage current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{OZL\text{-}min}$	Minimum pullup current	V_{IN} = GND; 50K pullup	-20	µA

Package Outline



Notice

The information contained in this document is believed to accurately represent the products described herein. However, Millogic Ltd (Millogic) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and documentation at any time without notice. Specifications are subject to change without notice.

Millogic warrants its products in accordance with the Millogic standard warranty. Testing and other quality control techniques are used to the extent Millogic deems necessary to support this warranty.

Millogic assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent or copyright to these products, and makes no representations or warranties that these products are free from patent, copyright infringement, unless otherwise specified.

Millogic Ltd.
6 Clock Tower Place
Maynard, MA 01754

http://www.millogic.com

For sales information, contact:

sales@millogic.com
978-461-1560